ALBEDO Telecom
Joan d'Austria, 112 - Barcelona - SP - 08018
Chalfont St Peter - Bucks - UK - SL9 9TR
www.albedotelecom.com

Ethernet Network Synchronization

Since early 2000 Telecommunication industry has moved from Time Multiplexig (TDM) or circuit-switched technology represented by PDH/SDH T-Carrier/SONET based to packet-switching or Statistical Multiplexing (STDM) represented by Ethernet and IP. It is what has been called network convergence or unification of all technologies around the Internet Protocol (IP).

Ethernet started as a LAN technology for enterprise networks, and is now being used in base station backhaul and aggregation networks, and even in metro networks. It turns out that many access network technologies such as PON require some kind of synchronization. This is also the case for all cellular mobile networks which require their base stations to be synchronized because it is fundamental to calculate de distance of every mobile that should really get synchronized simultaneouslty with the network. Both PON and Mobiles have some form of TDM in the access architecture therefore a good clock signal is required. Moreover, for Voice and Video/TV applications to manage properly the timing parameters -such as delay and jitter- under control is fundamental to get an acceptable Quality.

Ethernet was not designed to transport synchronization, then the problem is when Ethernet is used in aggregation and backhaul networks particularly when these technologies require any form of synchronization. This is the case of PON

Figure 1 *ALBEDO Ether.Sync is a field tester for Synchronous Ethernet equipped with all the features to install and maintain Precision Time Protocol (PTP / IEEE 1588v2), Synchronous Ethernet infrastructures, and Gigabit Ethernet supporting legacy features such as BER and RFC2544 while new test such as eSAM Y.1564.*

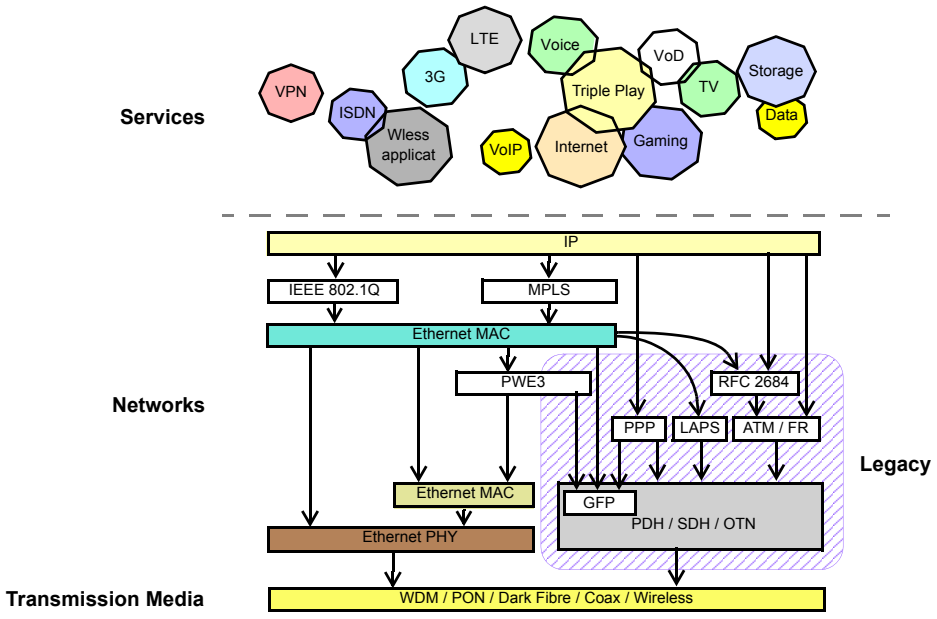

Figure 2 *Applications, Services and Protocols*

or GSM/3G/LTE networks. The answer is Synchronous Ethernet (SyncE) which simplifying is a traditional Ethernet plus an embeded synchronization transport feature ver similar to that already used in SDH/SONET.

SyncE enables the transport of synchronization signals has been standardized by the ITU-T, in cooperation with IEEE. Three recommendations have been published:

1. ITU-T Rec. G.8261 that defines aspects about the architecture and the wander performance of SyncE networks.
2. ITU-T Rec. G.8262 that specifies an equipment clock for SyncE, and G
3. ITU-T Rec. G.8264 that describes the specification of a synchronization signaling channel or ESMC (Ethernet Synchronization Messaging Channel).

Synchronization in Ethernet is not a simple topic and definetely be sure tha tis not something that can be understood by a simple replacement of the oscillator of the Ethernet card at the PHY layer with a Phase Locked Loop (PLL).

1. Network Convergence

IP and Ethernet, were selected a decade ago to build the Next Gen Networks. Both are based on statistical multiplexing, typical of packet technologies, has important advantages. The first is cost, as they are much cheaper to rollout

and maintain compared with circuit networks such as SONET/ SDH. The second: IP and Ethernet are easier to manage and have a lot of synergy with the Internet which is based on the same principals. But probably the ability to implement any new service based on voice, data and video is even more important than the benefits mentioned above.

IP is considered the best strategy to adopt in the deployment of the new converged services and, particularly television, which has for a long time been offered exclusively by cable, terrestrial and satellite operators. The IP protocol differentiates telco portfolios from competitors. Native IP-centric infrastructures that were developed for data transport, must be transformed into a multiservice platform that is also able to transport audio and video. To achieve this important investments are required.

The TCP/IP protocol, was designed in 1983 and immediately adopted by the US Department of Defense to connect heterogeneous hosts and has demonstrated itself to be very robust and suitable for managing large and complex topologies. It is also Internet-like and requires a minimum of human intervention. The Internet that we know, developed during the 1990s, is an architecture that provides universal connectivity between heterogeneous but open subsystems. TCP/IP protocols are designed to automatically locate topologies and addresses by means of nodes that are continuously interchanging routing information..

Table 1

Clock performance.

Type	*Performance*
Cesium	From 10^{-11} up to 10^{-13}
Hydrogen	From 10^{-11} up to 10^{-13}
GPS	Usually 10^{-12}
Rubidium	From 10^{-9} up to 10^{-10}
Crystal	From 10^{-5} up to 10^{-9}

IP & Ethernet

Ethernet scores high in a combination of features like efficiency, simplicity, scalability, and cost. It is also important that Ethernet is the technology used in the vast majority of customer premises and service provider installations. Ethernet is efficient as it is packet oriented, therefore it obtains the statistical multiplexing gain when transporting independent traffic flows over shared transmission medias. Ethernet is also very simple to set up and maintain especially when compared with SDH-SONET installations. Other important considerations are the number of engineers and technicians, probably millions, that are confident with Ethernet and all its associated devices and protocols such as switches and TCP/IP.

Ethernet is designed to be used with many types of optical and metallic media including the most popular. Transmission ranges and bandwidths are equivalent to long haul technologies. Being easily scalable from a few Mbit/s up to many Gbit/s (see Table 1.4) it is therefore possible to migrate existing LANs, MANs and WANs to Ethernet using the existing physical media

Ethernet drawbacks

Unfortunately, native Ethernet lacks some essential functions necessary to supply 'carrier-class' services. Features like reliability, management, rollout, maintenance and QoS are much more demanding in Metro networks supporting Triple Play than LANs where Ethernet is focused on data transport. Scalability can also be an issue. Ethernet switches work very well when the number of hosts connected is limited and during low traffic conditions, but as soon as the installation grows it tends to degrade in performance, QoS, security, availability. Moreover, the above mentioned lack of synchronization is an important limitation that has obligated to mantain the legacy synchronization system and signals like E1 / T1 and 2kHz as well.

When Ethernet is extended beyond the LAN, several architectures can fulfil the requirements including PON, Dark Fiber, DWDM / CWDM, NG-SDH. When deciding on which architecture to use most of these native Ethernet limitations are either forgotten either hidden which is worse.

Lack of synchronization

We mentioned about the need to keep delay and jitter under control but this can only be achieved if swithes/routers have short packet queues while minimize the packet loss. Fine, but to make it possible nodes should be synchronized to a unique clock reference.

So, What occurs if not? Well this is the case of today's Ethernet networks, each node has its own clock which always-always are slightly different, the consequence is that the buffer at that node will either overflow or underflow and packet will be lost or repeated to maintain a constant flow. This is a sample of *Bad synchronization* causes regeneration errors and *slips*. When this occurrs TCP types of data services, slips that occur force us to retransmit packets, and this makes not only the transmission less efficient but degrades the quality.

Digital Synchronization and Ethernet Switching

The frames are lined by means of a buffer in every input interface of a switch. The bits that arrive at f_i frequency get stored in them, to be read later at the frequency used by the switch, f_o.

But if the clocks are different, $|f_i - f_o| > 0$, the input buffer sooner or later ends up either empty or overloaded. This situation is known as a *slip*: If the buffer becomes empty, some bytes are repeated, whereas if the buffer is

overloaded, some valid bits must be discarded in order to continue working. That is to say, slips are errors that occur when PLLs cannot adapt themselves to clock differences or phase variations in framesin frames.

$$f_d = 86{,}000 \times |f_i - f_o| / n \qquad (\text{slips/day})$$

where
86,400 is number of seconds per day
n: bits repeated or discarded per slip
f_i = *input bit rate*
f_o = *output bit rate*

The effects of these impairments vary in different systems and services. Some isochronous services, like telephony, tolerate a deficient synchronization rather well, and small or no effects can be observed by the end-user. Others, like voice and video services, are more sensitive to synchronization problems.

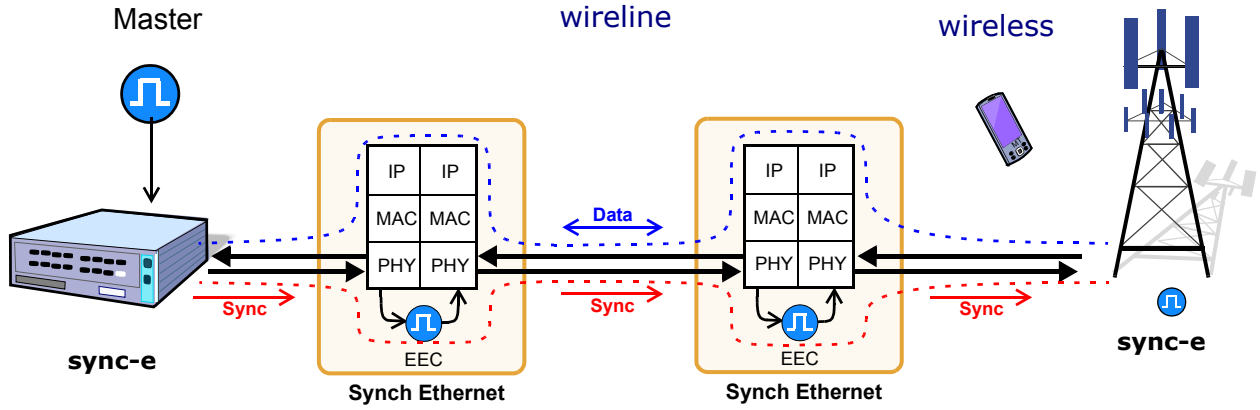

Figure 3 *In SynchE all internal clocks should be synchonized by a unique timing signal. The new Ethernet cards have an internal clock that is being synchronized by an external signal and transports the tim*

2. Architecture of Synchronization Networks

Synchronization networks can have hierarchical or nonhierarchical architectures. Networks that use *hierarchical synchronization* have a tree architecture. In such networks a master clock is distributed, making the rest of the clocks slaves of its signal (see Figure 4). A network with all the equipment clocks locked to a single master timing reference is called *synchronous*. The following elements can be found in the hierarchical synchronization network:

1. A *master clock*, which is usually an atomic cesium oscillator with global positioning system (GPS) and/or Loran-C reference. It occupies the top of the pyramid, from which many synchronization levels spread out (see Table 1).

2. High-quality *slave clocks*, to receive the master clock signal and, once it is filtered and regenerated, distribute it to all the NEs of their node.
3. *NE clocks,* which finish the branches of the tree by taking up the lowest levels of the synchronization chain. Basically, they are the ones using the clock, although they may also send it to other NEs.
4. *Links*, responsible for transporting the clock signal. They may belong to the synchronization network only, or, alternatively, form a part of a transport network, in which case the clock signal is extracted from data flow(see Figure 5).

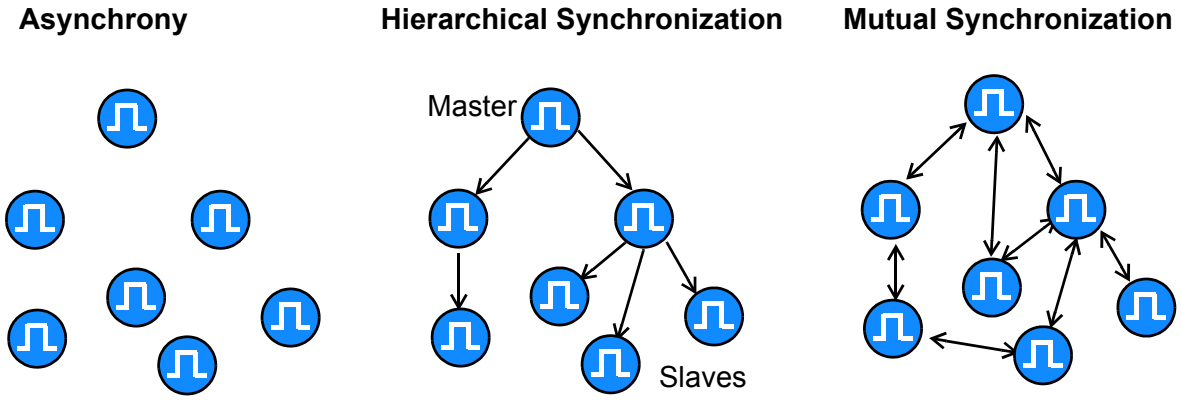

Figure 4 *Classes of synchronization architectures.*

The pure hierarchical synchronization architecture can be modified in several ways to improve network operation. *Mutual synchronization* is based on cooperation between nodes to choose the best possible clock. There can be several master clocks, or even a cooperative synchronization network, besides a synchronization protocol between nodes. Bringing these networks into services is more complex, although the final outcome is very solid.

Those networks where different nodes can use a clock of their own, and correct operation of the whole depends on the quality of each individual clock, are called *asynchronous*. Asynchronous operation can only be used if the quality of the node clocks is good enough, or if the transmission rate is reduced. The operation of a network (that may be asynchronous in the sense described above or not) is classified as *plesiochronous* if the equipment clocks are constrained within margins narrow enough to allow simple bit stuffing.

General requirements for today's Synchornous Ethernet networks are that any NE should have at least two reference clocks, of higher or similar quality than the clock itself. All the NEs must be able to generate their own synchronization signal in case they lose their external reference. If such is the case, it is said that the NE is in *holdover*.

A synchronization signal must be filtered and regenerated by all the nodes that receive it, since it degrades when it passes through the transmission path, as we will see later.

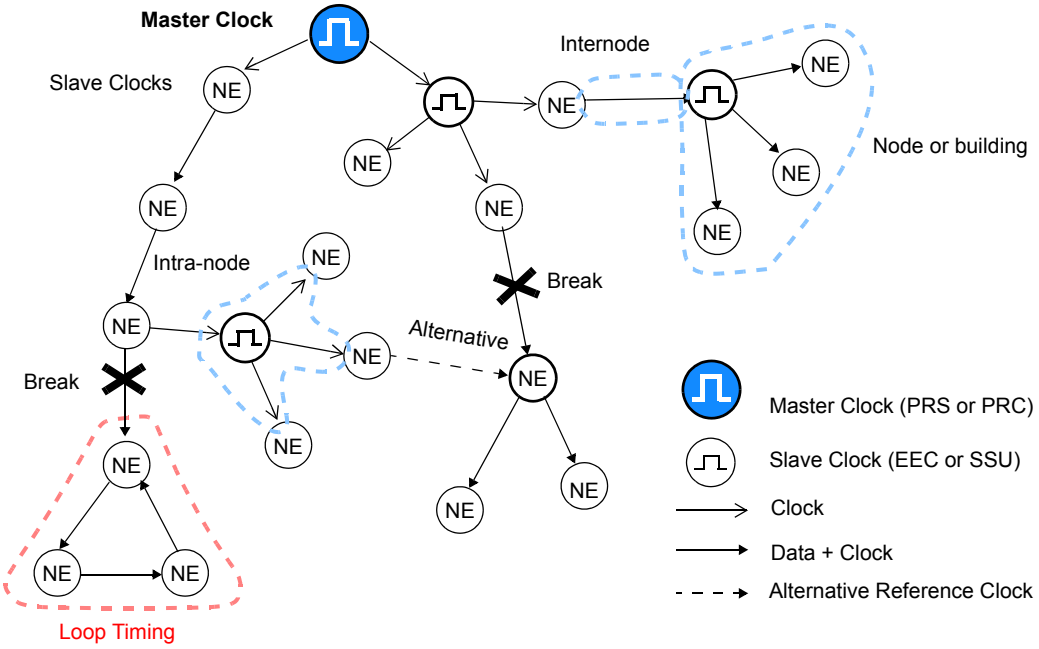

Figure 5 *Synchronization network topology for SynC Ethernet Architectures.*

Synchronization Network Topologies

The synchronization and transport networks are partially mixed, since some NEs both transmit data and distribute clock signals to other NEs.

The most common topologies are:

1. *Tree*: This is a basic topology that relies on a master clock whose reference is distributed to the rest of the slave clocks. It has two weak points: it depends on only one clock, and the signals gradually degrade(see Figure 7).
2. *Ring*: Basically, this is a tree topology that uses ring configurations to propagate the synchronization signal. The ring topology offers a way to make a tree secure, but care must be taken to avoid the formation of synchronizing loops.
3. *Distributed*: Nodes make widespread use of many primary clocks. The complete synchronization network is formed by two or more islands; each of them depending on a different primary clock. To be rigorous, such a network is asynchronous, but thanks to the high accuracy of the clocks commonly used as a primary clock, the network operates in a very similar way to a completely synchronous network.
4. *Meshed*: In this topology, nodes form interconnections between each other,

in order to have redundancy in case of failure. However, synchronization loops occur easily and should be avoided.

Synchronization networks used for Ethernet do not usually have only one topology, but rather a combination of all of them. Duplication and security involving more than one master clock, and the existence of some kind of synchronization management protocol, are important features of modern networks. The aim is to minimize the problems associated with signal transport, and to avoid depending on only one clock in case of failure. As a result, we get an extremely precise, redundant, and solid synchronization network.

3. Interconnection of Nodes

- There are two basic ways to distribute synchronization (see Figure 5):
- *Intranode*, which is a high-quality slave clock known as either *synchronization supply unit* (SSU) or *building integrated timing supply* (BITS). These are responsible for distributing synchronization to NEs situated inside the node.
- *Internode*, where the synchronization signal is sent to another node by a link specifically dedicated to this purpose, or by an PHY signal.

Synchronization Signals

There are many signals suitable for transporting synchronization:

- Analog, of 1,544 and 2,048 kHz
- Digital, of 1,544 and 2,048 Kbps
- SyncE signal at any bit rate
- STM-*n*/OC-*m* line codes

In any case, it is extremely important for the clock signal to be continuous. In other words, its mean frequency should never be less than its fundamental frequency (see Figure 6).

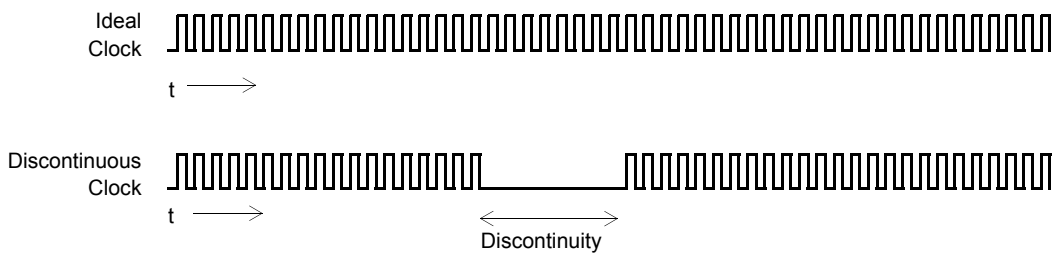

Figure 6 *A pure clock signal is continuous, as, for example, the one provided by an atomic clock.*

Clock transfer across Ethernet networks

These types of networks are not suitable for transmitting synchronization signals unless abslutely all the serie of nodes are SyncE. Important to emphatize that the signals never ever cross an Ethernet island not synchronized.

Clock transfer across T-carrier/PDH networks

These types of networks are very suitable for transmitting synchronization signals, as the multiplexing and demultiplexing processes are bit oriented (not byte oriented like SONET and SDH), and justification is performed by removing or adding single bits. As a result, T1 and E1 signals are transmitted almost without being affected by justification jitter, mapping or overhead-originated discontinuities. This characteristic is known as *timing transparency*.

There is only one thing to be careful with, and that is to not let T1 and E1 signals cross any part of SONET or SDH, as they would be affected by phase fluctuation due to mapping processes, excessive overhead, and pointer movements. It is probable that T1 or E1 will soon no longer be suitable.

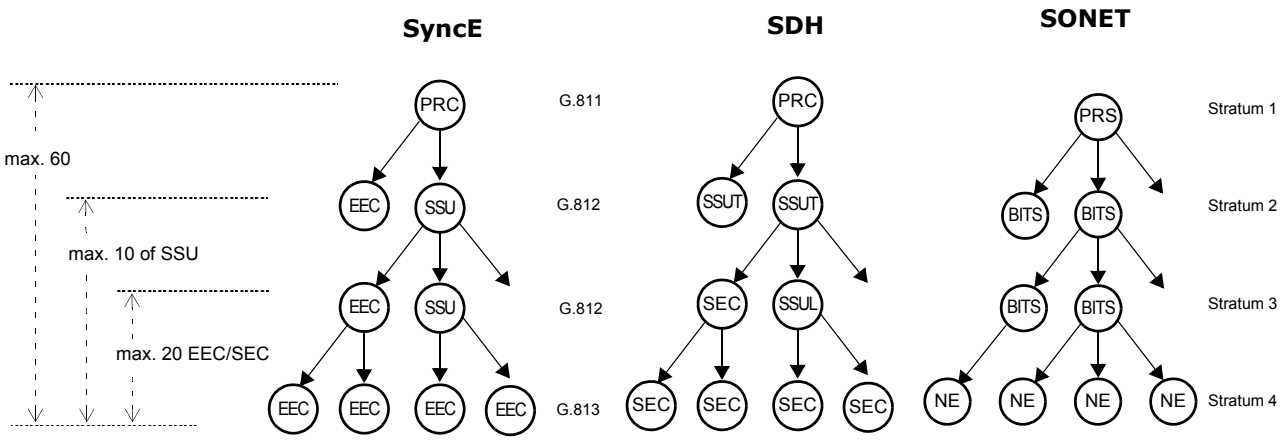

Figure 7 *Synchronization network model for Sync. Ethernet, SONET and SDH. In SDH the figures indicate the maximum number of clocks that can be chained together by one signal.*

Clock transfer across SDH/SONET links

To transport a clock reference across SDH/SONET, a line signal is to be used instead of the tributaries transported, as explained before. The clock derived from an STM-*n*/OC-*m* interface is only affected by wander due to temperature and environmental reasons. However, care must be taken with the number of NEs to be chained together, as all the NEs regenerate the STM-*n*/OC-*m* signal with their own clock and, even if they were well synchronized, they would still cause small, accumulative phase errors.

The employment of STM-*n*/OC-*m* signals has the advantage of using the S1 byte to enable *synchronization status messages* (SSMs) to indicate the performance of the clock with which the signal was generated(see Figure 8). These messages are essential in reconstructing the synchronization network automatically in case of failure. They enable the clocks to choose the best possible reference, and, if none is available that offers the performance required, they enter the holdover state.

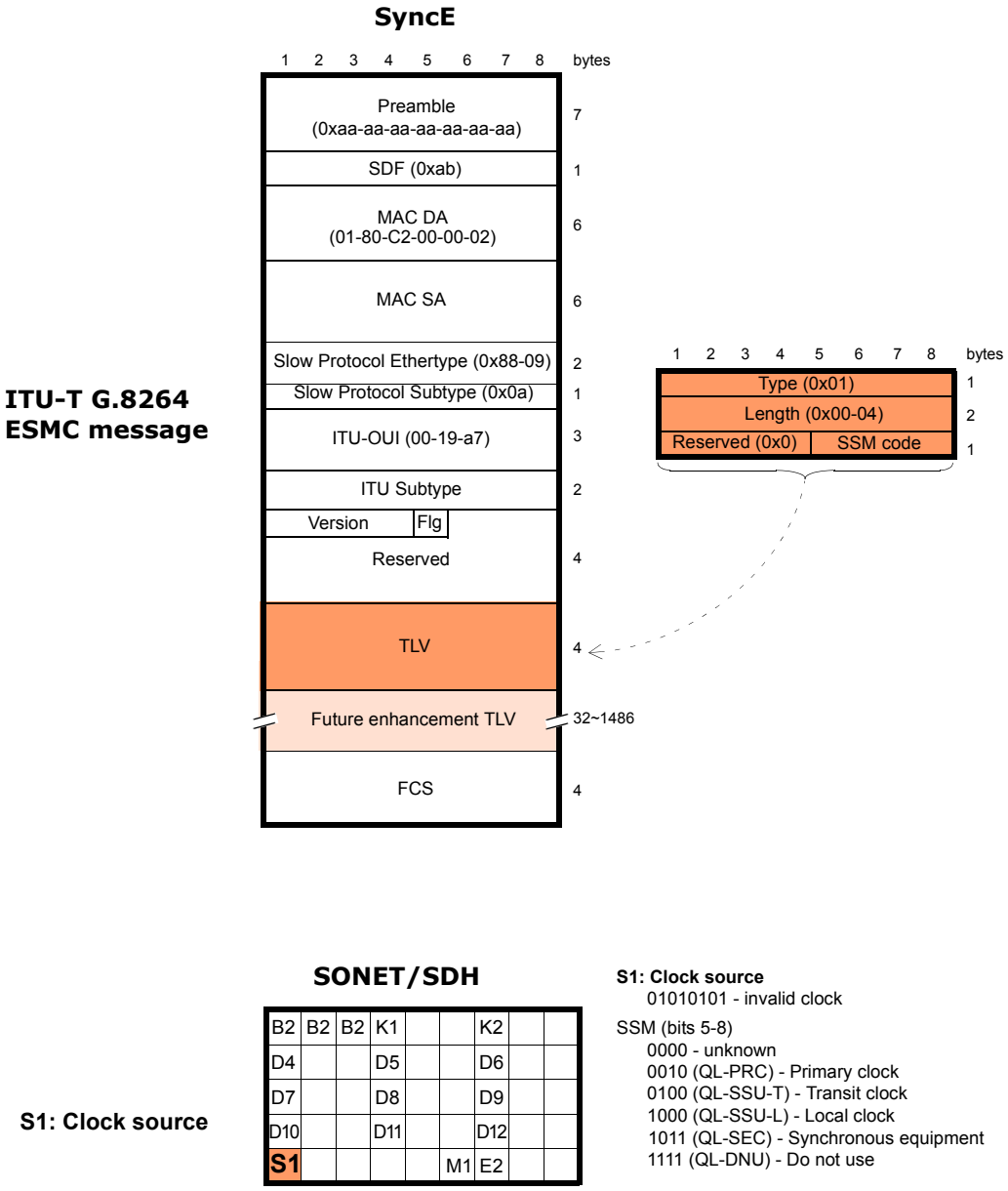

Figure 8 *Ethernet Synchronization Message Channel (ESMC) protocol data unit rec. ITU-T G.8264.*

Holdover Mode

It is said that a slave clock enters holdover mode when it decides to use its own generator, because it does not have any reference available, or the ones available do not offer the performance required. In this case, the equipment remembers the phase and the frequency of the previous valid reference, and reproduces it as well as possible.

Global Positioning System

The *global positioning system* (GPS) is a constellation of 24 satellites that belongs to the U.S. Department of Defense. The GPS receivers can calculate, with extreme precision, their terrestrial position and the universal time from where they extract the synchronization signal. The GPS meets the performance required from a primary clock (see Table 1). However, the GPS system might get interfered with intentionally, and the U.S. Department of Defense reserves the right to deliberately degrade it for tactical reasons.

4. Disturbances in Synchronization Signals

Since synchronization signals are distributed, degradation in the form of jitter and wander accumulate. At the same time they are affected by different phenomena that cause phase errors, frequency offset, or even the complete loss of the reference clock. Care must be taken to avoid degradation in the form of slips and bit errors by filtering and an adequate synchronization distribution architecture(see Figure 9).

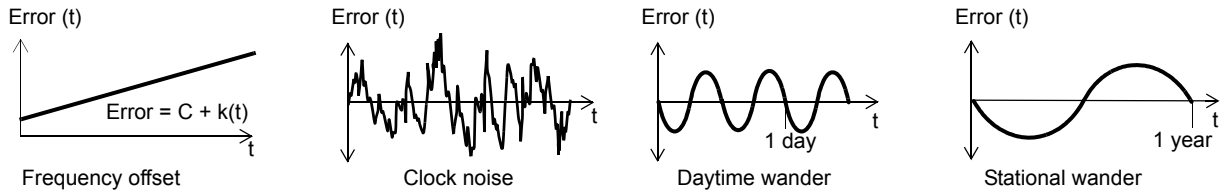

Figure 9 *Sources of phase variation.*

Frequency Offset

Frequency offset is an undesired effect that occurs during the interconnection of networks or services whose clocks are not synchronized. There are several situations where frequency deviations occur (see Figure 9):

- On the boundary between two synchronized networks with different primary reference clocks

- When tributaries are inserted into a network by nonsynchronized ADMs
- When, in a synchronization network, a slave clock becomes disconnected from its master clock and enters holdover mode.

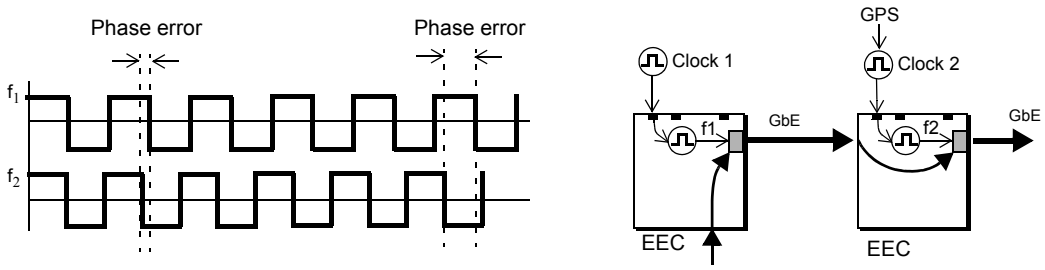

Figure 10 *Comparison of two reference signals that synchronize two Ethernet nodes.*

Phase Fluctuation

In terms of time, the phase of a signal can be defined as the function that provides the position of any significant instant of this signal. It must be noticed that a time reference is necessary for any phase measurement, because only a phase relative to a reference clock can be defined. A significant instant is defined arbitrarily; it may for instance be a trailing edge or a leading edge, if the clock signal is a square wave (see Figure 11).

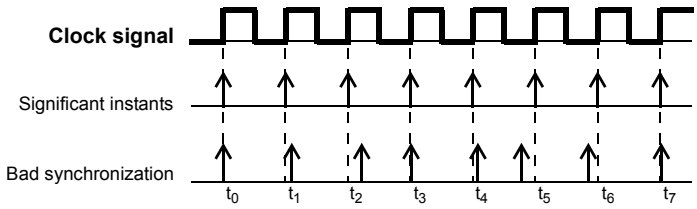

Figure 11 *Phase error of a signal in relation to its ideal frequency.*

Here, when we talk about a phase, we think of it as being related to clock signals. Every digital signal has an associated clock signal to determine, on reception, the instants when to read the value of the bits that this signal is made up of. The clock recovery on reception circuits reads the bit values of a signal correctly when there is no phase fluctuation, or when there is very little. Nevertheless, when the clock recovery circuitry cannot track these fluctuations (absorb them), the sampling instants of the clock obtained from the signal may not coincide with the correct instants, producing bit errors.

When phase fluctuation is fast, this is called jitter. In the case of slow phase fluctuations, known as wander, the previously described effect does not occur. Phase fluctuation has a number of causes. Some of these are due to imperfections in the physical elements that make up transmission networks, whereas others result from the design of the digital systems.

Jitter

Jitter is defined as short-term variations of the significant instants of a digital signal from their reference positions in time, ITU-T Rec. G.810(see Figure 13). In other words, it is a phase oscillation with a frequency higher than 10 Hz. Jitter causes sampling errors and provokes slips in the *phase-locked loops* (PLL) buffers(see Figure 14). There are a great many causes, including the following:

Jitter due to packetising

Analog phase variation in payload signals is sampled and quantized when these are multiplexed in a higher-order signal. Also, a payload could be synchronized with a different clock than the clock used to synchronize the aggregate signal that will carry it.

Wander

Wander is defined as long-term variations of the significant instants of a digital signal from their reference positions in time (ITU-T Rec. G.810). Strictly speaking, wander is defined as the phase error comprised in the frequency band between 0 and 10 Hz of the spectrum of the phase variation. Wander is difficult to filter when crossing the *phase-locked loops* (PLLs) of the SSUs, since they hardly attenuate phase variations below 0.1 Hz.

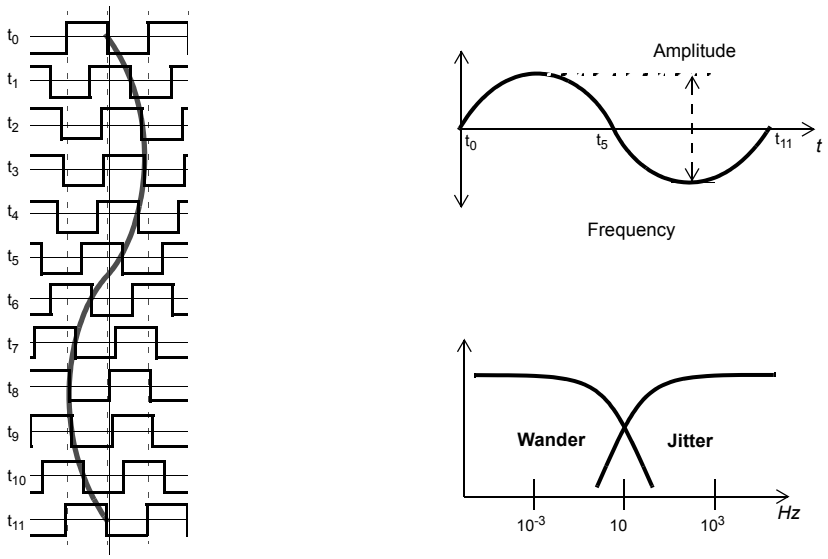

Figure 12 *A phase fluctuation of a signal is an oscillating movement with an amplitude and a frequency. If this frequency is more than 10 Hz, it is known as jitter, and when it is less than that, it is called wander.*

Wander brings about problems in a very subtle way in a chained sequence of events that are then reflected in other parts of the network in the form of jitter. This in its turn ends up provoking slips in the output buffers of the transported tributary.

The following are the most typical causes of wander:

Changes in temperature

Variations between daytime and nighttime temperature, and seasonal temperature changes have three physical effects on transmission media:

- There are variations in the propagation rate of electrical, electromagnetic or optical signals.
- There is variation of length, when the medium used is a cable (electrical or optical), due to changes between daytime and nighttime or winter/summer.
- There is different clock behavior when temperature changes occur.

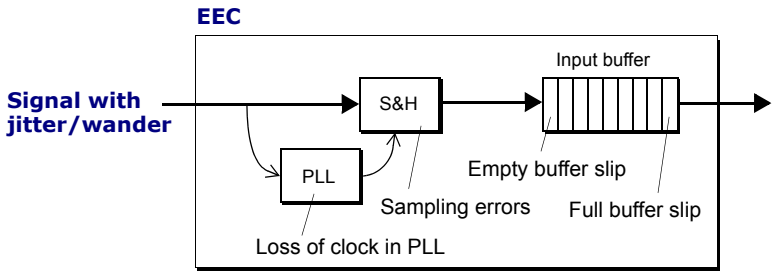

Figure 13 *Jitter & wander affect every stage of data recovery, producing sampling errors, clock, losses, and overflow.*

Clock performance

Clocks are classified according to their average performance in accuracy and offset. The type of resonant oscillator circuit used in the clock source and the design of its general circuitry both add noise, and this results in wander.

5. SYNCHRONIZATION OF TRANSMISSION NETWORKS

T-carrier and PDH networks have their first hierarchy perfectly synchronous. In E1 and DS1 frames, all the channels are always situated in their own timeslots. The rest of the hierarchical multiplexion levels are not completely synchronous, but frequency differences can be accommodated by the bit stuffing mechanism.

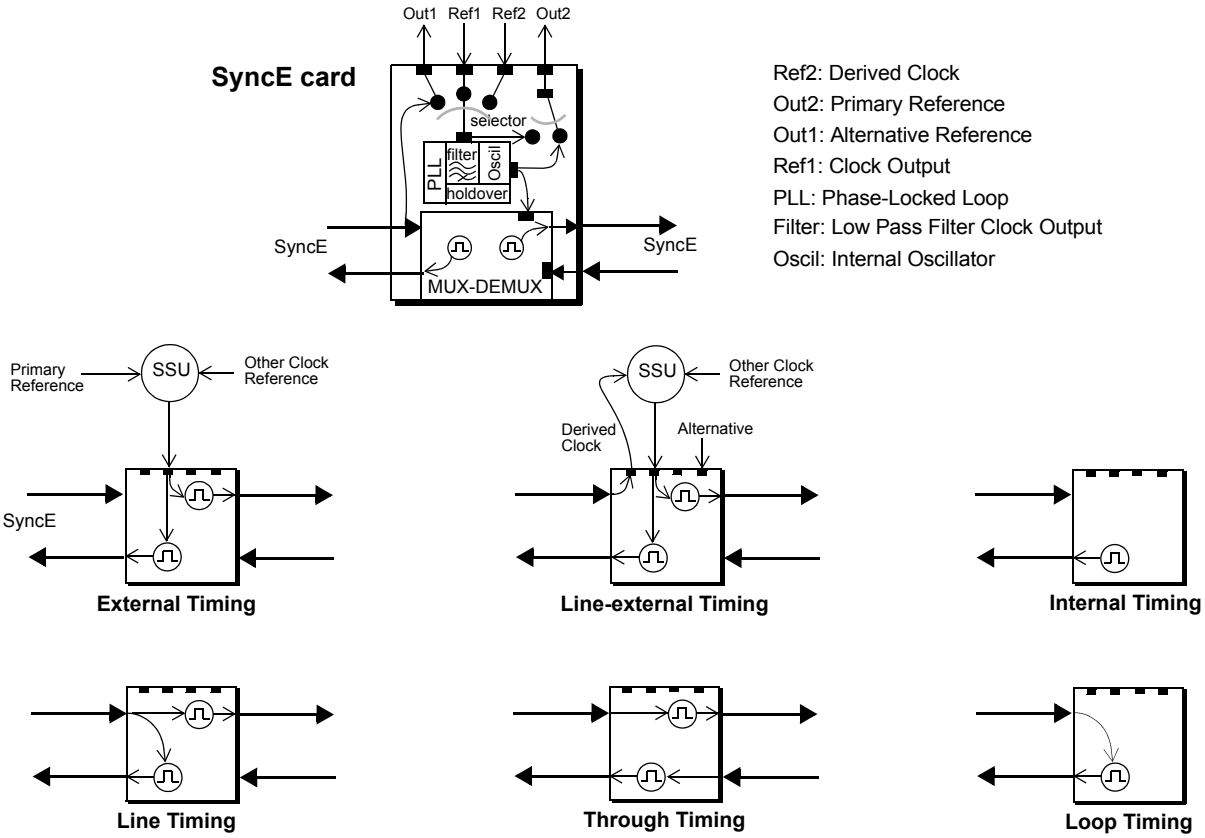

Figure 14 *Synchronization models of Synchronous Ethernet switches*

T-carrier and PDH nodes do not need to be synchronized, since each of them can maintain their own clock. The only requirement is that any clock variations must be kept within the specified limits, so that the available justification bits can be fitted in without problems caused by clock differences.

Synchronization in SONET and SDH

In SONET and SDH, the NEs must be synchronized to reduce pointer movements to a minimum. Pointer movements, as we have seen, are a major cause of jitter. The synchronization network follows a master-slave hierarchical structure:

- *Primary reference clock,* in SDH, or *primary reference source,* in SONET: This is the one that provides the highest quality clock signal. It may be a cesium atomic clock, or a *coordinated universal time* (UTC) signal transmitted via the GPS system.
- *Synchronization supply unit,* in SDH, or *building integrated timing supplies,* in SONET: This clock takes its reference from the PRC and provides timing to the switching exchanges and NEs installed in the same building (it is also known as *building synchronization unit*) or on the same premises. It is usually an atomic clock, although not of such a high quality as the PRC.

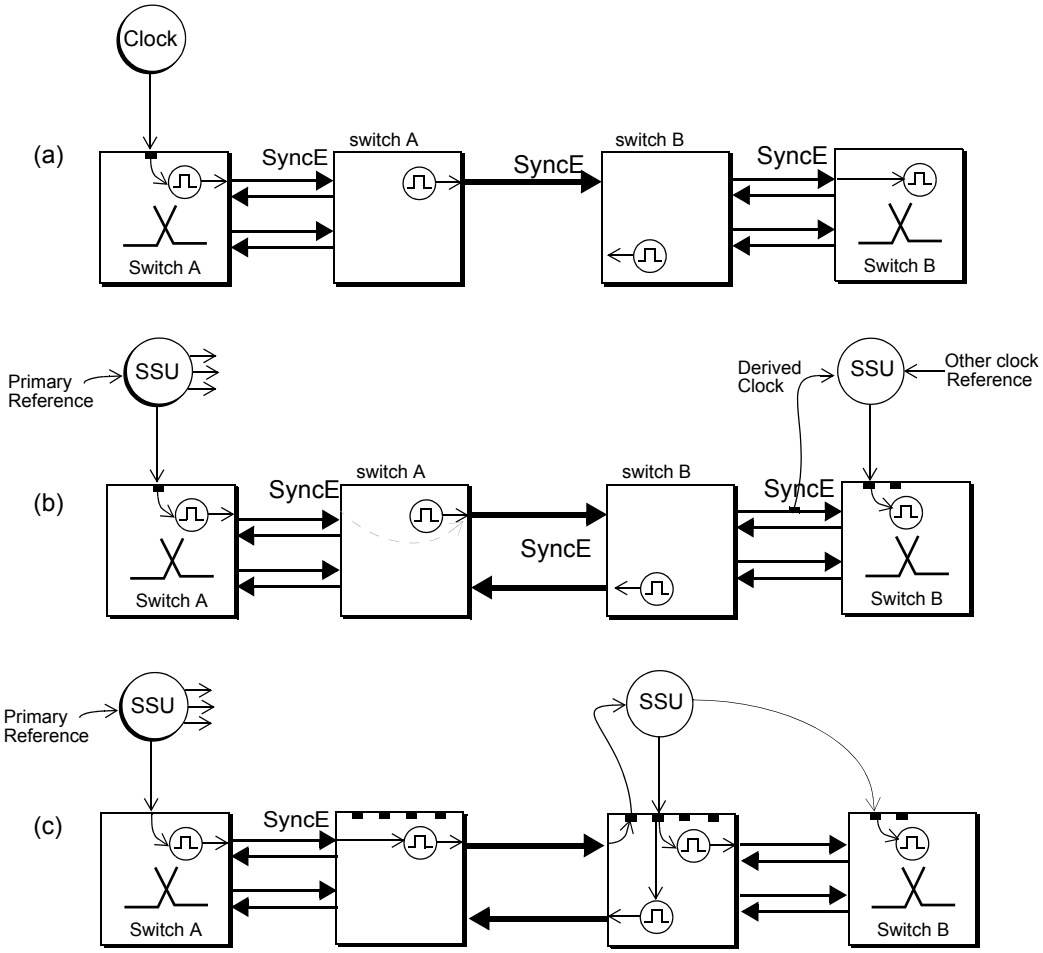

Figure 15 *Synchronization of two digital centrals: (a) by signal derived from the SyncE chain; (b) by external reference and SSU chain; and (c) across SyncE network.*

- *Synchronous equipment clock* (SEC): This clock takes its reference from an SSU, although it is of lower quality (for example, quartz). It is the internal clock of all the NEs (multiplexer, ADM, etc.).

  Whereas a PRC/PRS clock is physically separate from the SDH/SONET network, an SSU/BITS clock may be a separate piece of equipment, in which case it is called a *stand-alone synchronization equipment*, or it may be integrated into an NE (DXC or multiplexer). By definition, an SEC is integrated into an NE. The timing between clocks is transmitted by SDH/SONET sections (STM-*n*/OC-*m*) or PDH/T-carrier paths (2 or 1.5 Mbps) that can cross various intermediary PDH/T-carrier multiplexing stages, and various PDH/T-carrier line systems. The interfaces for these clocks are 2 or 1.5 Mbps, 2 or 1.5 MHz and STM-*n*/OC-*m*, and their presence or absence depends on the specific implementation of the device.

SONET synchronization network

In a SONET synchronization network, the master clock is called *primary reference source* (PRS), whereas slave clocks are building integrated timing supply (BITS) that end up synchronizing the NEs. The GR-1244-CORE specifies the rules and performance margins for both PRS and BITS.

BITS synchronizes the network equipment, and it is also used by switches. The performance required to synchronize a node is Stratum 3.

SDH synchronization network

In an SDH synchronization network, the master clock is called *primary reference clock* (PRC), whereas *synchronization supply units* (SSUs) are slave clocks and the NE is a *synchronous equipment clock* (SEC). All of them must be kept inside the performance margins defined by the corresponding recommendations (see Table 3).

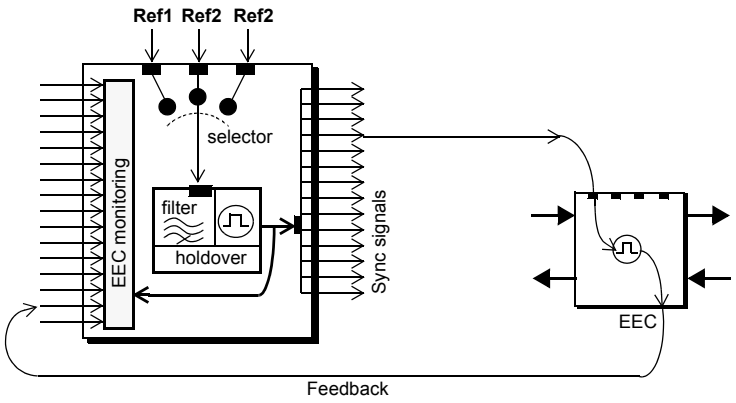

Figure 16 *Diagram of an SSU function model synchronizing and Ethernet node.*

Synchronization Models

In SyncE, there are several ways to synchronize nodes (see Figure 14):

1. *External timing*: The EEC obtains its signal from an *stand-alone synchronization equipment* (SASE). This is a typical way to synchronize, and the NE usually also has an extra reference signal for emergency situations.
2. *Line timing*: The NE obtains its clock by deriving it from one of the input signals. This is used alternative clock is available.
3. *Through timing*: Where the Tx outputs of one interface are synchronized with the Rx inputs of the opposite interface.
4. *Internal timing*: In this mode, the internal clock of the EEC is used to synchronize outputs. It may be a temporary holdover stage after losing the synchronization signal, or it may be a simple line configuration where no other clock is available.

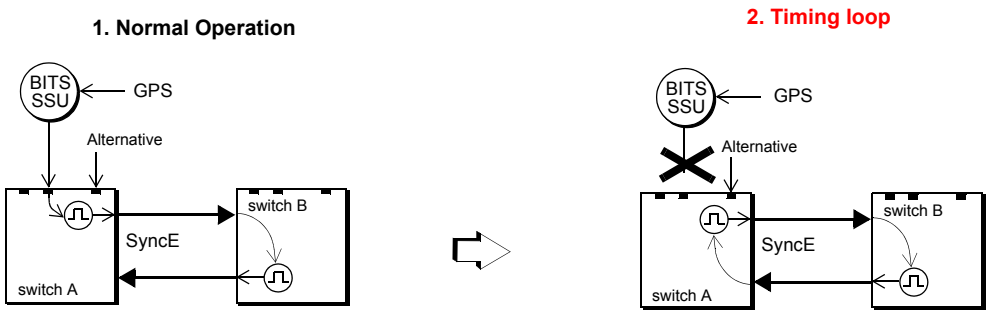

Figure 17 *A synchronization pitfall. The switch A, when left without a reference, should have remained in holdover, if it did not have another clock signal. Secondary clock references should not be taken in line timing.*

Timing Loops

A timing loop is in bad synchronization when the clock signal has closed itself, but there is no clock, either master or slave, that would autonomously generate a nondeficient clock signal. This situation can be caused by a fault affecting an NE in such a way that it has been left without a reference clock, and therefore it has chosen an alternative synchronization: a signal that has turned out to be the same signal, returning by another route (see Figure 17). A synchronization loop is a completely unstable situation that may provoke an immediate collapse of part of the network within the loop.

6. SSU IN A SYNCHRONIZATION NETWORK

The SSU is in charge of synchronizing all the SyncE switches of its location. It has several clock references, to confront possible clock signal losses.

Functions of SSU

An SSU has many functions, and they can be described as follows:

1. The SSU accepts many clock references, tests their performance and selects one of them, filtering it from noise and other interference.
2. It sends the signal chosen to an internal oscillator that acts as a reference to generate a new synchronization signal.
3. The new signal is distributed between all the NEs of its node, and it may also be sent to another SSU in another node.
4. If the reference chosen starts to degrade or is lost, the SSU should switch to one of its alternative references.
5. If no valid reference is found, the SSU enters holdover mode, generating a clock of its own that emulates the previous valid reference.

ALBEDO Telecom

ALBEDO Telecom designs, manufactures, and delivers solutions that enable Telecom organizations of all sizes to test, measure, troubleshoot, monitor, and migrate mission critical networks and multiplay applications.

On local segments and across distributed networks, ALBEDO enable Organizations, Installers, Operators, Service Providers and Suppliers to quickly check the health of Network Architectures, Service Agreements (SLA), IP Quality (QoS), or fix any issue.

Your Business Partner

Results. ALBEDO Telecom helps the industry to make the most of the investment on infrastructure.

Expertise. ALBEDO Telecom engineers and consultants provide industry leading knowledge in hand-held TAPs and WAN emulators, IPTV, VoIP, Carrier-Ethernet, Synchronization, Jitter, Wander, SyncE, PTP, E1, and Datacom to address customers unique needs.

Integration. ALBEDO Telecom integrates disparate telecom technologies and applications, facilitating new business efficiencies.

Agility. ALBEDO Telecom increases the ability of customers to respond quickly to new market opportunities and requirements.

Coverage. ALBEDO Telecom offers solutions that facilitates the migration and the roll-out to new architectures.

ALBEDO Telecom

the Path to Excellence

Joan d'Austria, 112 - Barcelona - 08018 - SP
Chalfont St Peter - Bucks - SL9 9TR - UK
www.albedotelecom.com

aims

+ UNDERSTAND causes of telecom interoperability issues
+ EXPERIENCE the best quality in unified networking
+ ASSESS different hardware, firmware, and software solutions
+ LEARN from experts by means of professional services and consultancy